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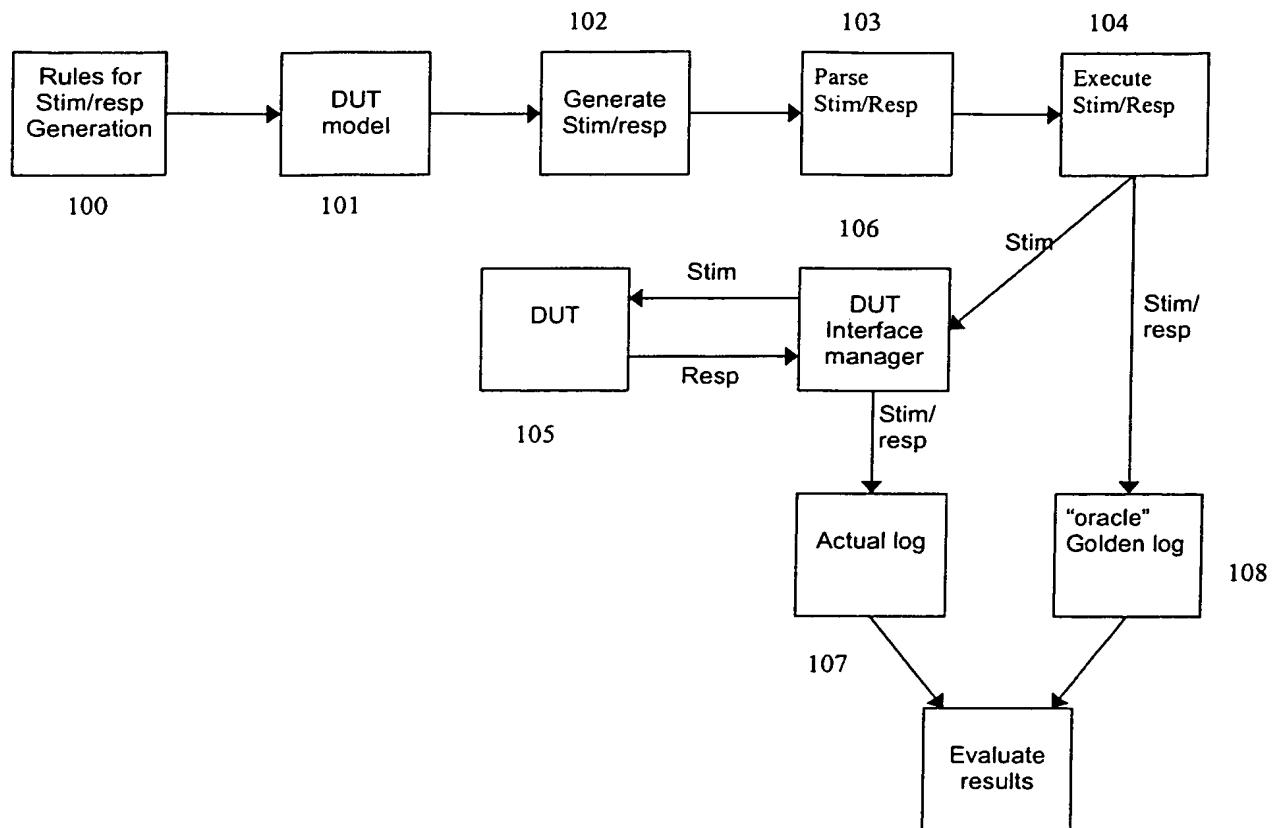


Fig 1

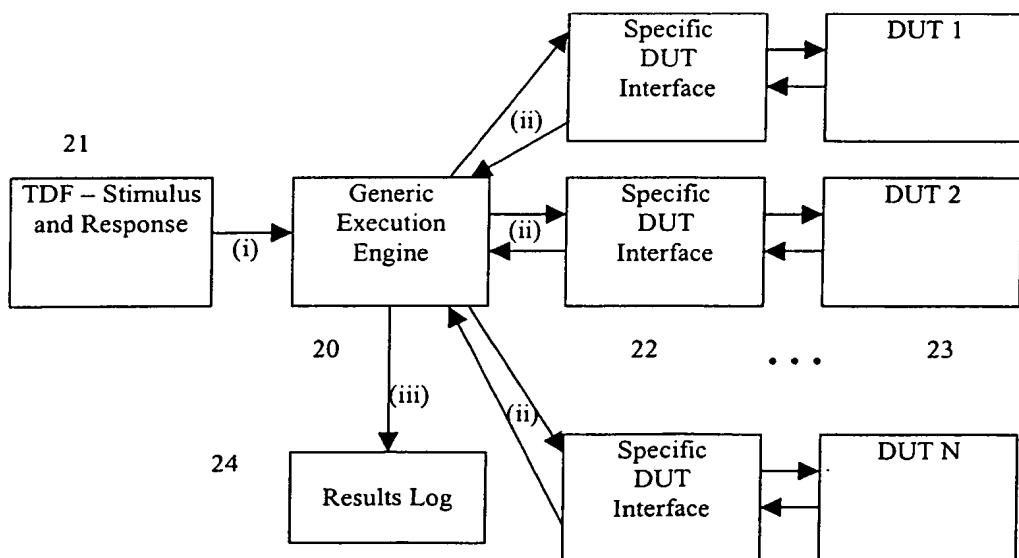
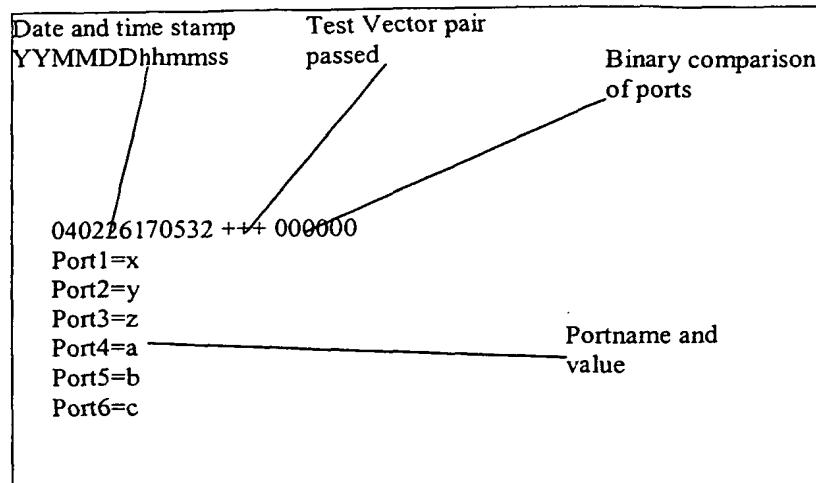
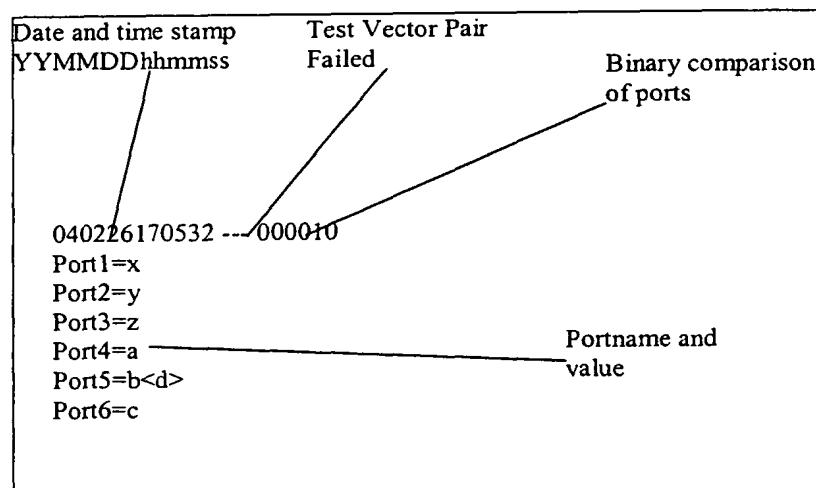
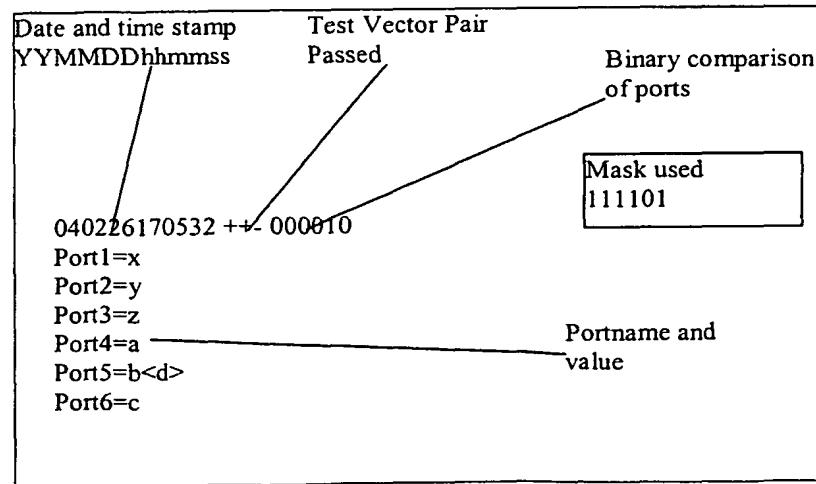


Figure 2 Generic Execution Engine Architecture

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**Fig 3a****Fig 3b****Fig 3c**

Input Port1	Input Port2	Input Port3	Output Port4	Output Port5	Output Port6
x_1	y_1	z_1	a_1	b_1	c_1
x_2	y_2	z_2	a_2	b_2	c_2
x_3	y_3	z_3	a_3	b_3	c_3
x_n	y_n	z_n	a_n	b_n	c_n

Fig 4